IN THE SPECIFICATION:

Page 1, before "BACKGROUND OF THE INVENTION, insert the following:

--This is a continuation application of Application No. 09/330,153, filed on June 11, 1999.--.

Please substitute the following paragraph for the paragraph starting at page 4, line 5 and ending at line 10.

Known examples of the FE type electron-emitting devices are described in W.P. Dyke and W.W. Dolan, "Field ~~emission",~~ emission," Advance in Electron Physics, 8, 89 (1956) and C.A. Spindt, "Physical properties of thin-film ~~film-film~~ field emission cathodes with molybdenium ~~cones",~~ cones," J. Appl. Phys., 47, 5248 (1976).

Please substitute the following paragraph for the paragraph starting at page 6, line 8 and ending at line 23.

Particularly as an application to image display apparatuses, as disclosed in the U.S. Patent No. ~~5,066,833~~ 5,066,883 and Japanese Patent Laid-Open Nos. 2-257551 and 4-28137 filed by the present applicant, an image display apparatus using the combination of a surface-conduction emission type electron-emitting device and a fluorescent substance which emits light upon irradiation of an electron beam has been studied. This type of image display apparatus using the combination of the surface-conduction emission type electron-emitting device and the fluorescent substance is expected to exhibit more excellent characteristics than other conventional image display apparatuses. For example, compared with recent popular liquid crystal display apparatuses, the above display apparatus is superior in that it does not require any backlight because it is of a self-emission type and that it has a wide view angle.

Please substitute the following paragraph for the paragraph starting at page 8, line 13 and ending at page 9, line 17.

In a multi electron source constituted by arranging surface-conduction emission type electron-emitting devices in a simple matrix, appropriate electrical signals are applied to the row- and column-direction wirings 4002 and 4003 to output a desired electron beam. For example, to drive the surface-conduction emission type electron-emitting devices on an arbitrary row in the matrix, a selection potential Vs is applied to the row-direction ~~column-direction~~ wiring 4002 on a selected row, and at the same time a non-selection potential Vns is applied to the row-direction wirings 4002 on an unselected row. In synchronism with this, a driving potential Ve for outputting an electron beam is applied to the column-direction wiring 4003. According to this method, when voltage drops across the wiring resistances 4004 and 4005 are neglected, a voltage (Ve - Vs) is applied to the surface-conduction emission type electron-emitting devices on the selected row, while a voltage (Ve - Vns) is applied to the surface-conduction emission type electron-emitting devices on the unselected row. When the potentials Ve, Vs, and Vns are set to appropriate magnitudes, an electron beam having a desired intensity must be output from only the surface-conduction emission type electron-emitting devices on the selected row. When different driving voltages Ve are applied to respective column-direction wirings, electron beams having different intensities must be output from the respective devices on the selected row. Since the surface-conduction emission type electron-emitting device has a high response speed, a change in length of time for which the driving voltage Ve is applied necessarily causes a change in length of time for which an electron beam is output.

Please substitute the following paragraph for the paragraph starting at page 23, line 24 and ending at page 24, line 26.

The A/D converter 3 converts an analog video luminance signal into n serial digital signals per horizontal period, and outputs the digital signals. These digital signals are sent to and held by a horizontal shift register 6 where they are converted into parallel signals, and sent to and stored in a l-line memory 7. A column wiring driver 10 comprises, in units of column

wirings, current sources I1 each for applying a current to a corresponding column wiring via a switching circuit 103 when an output pulse signal from a PWM generator 101 (to be described below) corresponding to input luminance data is ON, transistors 100 each for driving a corresponding column wiring by a current limited by a current source I2 via the switching circuit 103 when luminance data is OFF, and PWM generators (PWM ~~PWN~~ GEN) 101 each for outputting a signal having a pulse width proportional to luminance data for turning on/off the transistor 100. The switching circuit 103 flows a current from the current source I1 to a column wiring when a pulse signal (luminance data) from the PWM generator (PWM ~~PWN~~ GEN) 101 is at high level, and connects the column wiring to the transistor 100 when the pulse signal changes to low level. The column wiring driver 10 also comprises diodes 102 each for clipping a column wiring application potential to Vm, as protection means for preventing a potential applied to the device from exceeding the rated value when luminance data is at high level. Note that a potential Vas connected to the current source I2 of the column wiring driver 10 may be at ground level or about several negative V, and a potential Vdd is almost equal to the potential Ve in Fig. 3.

Please substitute the following paragraph for the paragraph starting at page 26, line 10 and ending at page 26, line 14.

In this example, the pulse rise time is long owing to driving by the current source I1, The same effects can be attained even for a short driving signal rise time when, ~~when,~~ for example, the voltage source is used for driving up to a given potential, and then the current source operates.

Please substitute the following paragraph for the paragraph starting at page 30, line 24 and ending at page 31, line 13.

Furthermore, a metal back 1009, which is well-known in the CRT field, is provided on the fluorescent film 1008 on the rear plate side. The purpose of providing the metal back 1009 is to improve the light-utilization ratio by mirror-reflecting part of the light emitted by

the fluorescent film 1008, to protect the fluorescent film 1008 from collision with negative ions, to be used as an electrode for applying an electron accelerating voltage, to be used as a conductive path for electrons which excited the fluorescent film 1008, and the like. The metal back 1009 is formed by forming the fluorescent film 1008 on the face plate substrate 1007, smoothing the front surface on the fluorescent film , and depositing aluminum thereon by vacuum deposition. Note that when fluorescent substances for a low voltage are ~~is~~ used for the fluorescent film 1008, the metal back 1009 is not used.

Please substitute the following paragraph for the paragraph starting at page 32, line 17 and ending at page 33, line 18.

A method of manufacturing the multi electron source used in the display panel 1000 of this embodiment will be described below. In the multi electron source used in the image display apparatus of this embodiment, any material, shape, and manufacturing method for cold cathode ~~device~~ devices may be employed as long as the electron source is constituted by arranging surface-conduction emission type electron-emitting devices in a simple matrix. Therefore, cold cathode devices such as surface-conduction emission type electron-emitting devices, FE type devices, or MIM type devices can be used. However, the present inventors have found that among the surface-conduction emission type electron-emitting devices, an electron source having an electron-emitting portion or its peripheral portion consisting of a fine particle film is excellent in electron-emitting characteristic and can be easily manufactured. Such a device can therefore be most suitably used for the multi electron source of a high-brightness, large-screen image display apparatus. For this reason, in the display panel of this embodiment, surface-conduction emission type electron-emitting devices each having an electron-emitting portion or its peripheral portion made of a fine particle film are used. The basic structure, manufacturing method, and characteristics of the preferred surface-conduction emission type electron-emitting device will be described first. The structure of the multi electron source having many devices arranged in a simple matrix will be described later.

Please substitute the following paragraph for the paragraph starting at page 35, line 1 and ending at line 9.

The shape of the electrodes 1102 and 1103 is appropriately designed in accordance with an application object of the electron-emitting device. Generally, an interval L between electrode is designed by selecting an appropriate value in a range from hundred Å to hundred ~~μm~~ μm. Most preferable range for a display apparatus is from several μm to ten μm. As for electrode thickness d, an appropriate value is selected in a range from hundred Å to several μm.

Please substitute the following paragraph for the paragraph starting at page 37, line 8 and ending at page 37, line 12.

The thin film 1113, which comprises carbon or carbon compound material, covers the electron-emitting portion 1105 ~~1115~~ and its peripheral portion. The thin film 1113 is formed by the activation processing to be described later after the forming processing.

Please substitute the following paragraph for the paragraph starting at page 42, line 23 and ending at page 43, line 16.

In Fig. 10D, reference numeral 1114 denotes an anode electrode, connected to a DC high-voltage power source 1115 and galvanometer 1116, for capturing emission current Ie emitted from the surface-conduction emission type electron-emitting device. (In the case in which the substrate 1101 is incorporated into the display panel before the activation processing, the fluorescent surface of the display panel is used as the anode electrode 1114.) While applying voltage from the activation power source 1112, the galvanometer 1116 measures the emission current Ie, thus monitoring ~~monitors~~ the progress of activation processing, to control the operation of the activation power source 1112. Fig. 12B shows an example of the emission current Ie measured by the galvanometer 1116. As application of pulse voltage from the activation power source 1112 is started in this manner, the emission current Ie increases with

elapse of time, gradually comes into saturation, and almost never increases then. At the substantial saturation point, the voltage application from the activation power source 1112 is stopped, then the activation processing is terminated.

Please substitute the following paragraph for the paragraph starting at page 49, line 18 and ending at page 50, line 6.

Fig. 18 is a block diagram showing an example of a multi-functional display apparatus capable of displaying image information provided from various image information sources such as television broadcasting on a display panel using the surface-conduction emission type electron-emitting device of this embodiment as an electron-beam source. Referring to Fig. 18, reference numeral 2100 ~~1000~~ denotes the above-mentioned display panel; 2101, a driving circuit for the display panel; 2102, a display controller; 2103, a multiplexer; 2104, a decoder; 2105, an I/O interface circuit; 2106, a CPU; 2107, an image generation circuit; 2108, 2109, and 2110, image memory interface circuits; 2111, an image input interface circuit; 2112 and 2113, TV signal reception circuits; and 2114, an input portion.

Please substitute the following paragraph for the paragraph starting at page 55, line 9 and ending at line 12.

The driving circuit 2101 generates a driving signal to be applied to the display panel 2100 ~~1000~~, and operates based on an image signal input from the multiplexer 2103 and a control signal input from the display panel controller 2102.

Please substitute the following paragraph for the paragraph starting at page 55, line 13 and ending at page 56, line 17.

The functions of the respective parts have been described. The arrangement of the display apparatus shown in Fig. 18 makes it possible to display image information input from various image information sources on the display panel 2100 ~~1000~~. More specifically, various

image signals such as television broadcasting image signals are inversely converted by the decoder 2104, appropriately selected by the multiplexer 2103, and supplied to the driving circuit 2101. On the other hand, the display controller 2102 generates a control signal for controlling operation of the driving circuit 2101 in accordance with an image signal to be displayed. The driving circuit 2101 applies a driving signal to the display panel 2100 ~~1000~~ on the basis of the image signal and control signal. As a result, the image is displayed on the display panel 2100 ~~1000~~. A series of operations are systematically controlled by the CPU 2106.

Please delete the following paragraph starting at page 61, line 15 and ending at line 16.

~~In this way, the third embodiment can preferably modulate the pulse width with a simple circuit.~~

Please substitute the following paragraph for the paragraph starting at page 74, line 16 and ending at page 75, line 2.

In Fig. 34, reference numeral 70 denotes a voltage source for outputting the potential Vas [V]; 71, an input terminal for inputting a modulated signal (~~XDPi: i = 1~~ XDPJ: j = 1 to 480) from the modulated-signal generator 10006; 72, a current source for driving the cold cathode device of the matrix type display panel 10001 and displaying an image; 73, a diode; 74, an inverter circuit; 75, a transistor such as a MOSFET for controlling whether or not to supply a driving current from the current source 72 to the display panel 10001; 76, a 3-input OR circuit; 77, a level shift circuit; 78, an NPN transistor for controlling whether or not to apply the potential Vas to the modulated-signal wiring of the display panel 10001; and 79, a diode.

Please substitute the following paragraph for the paragraph starting at page 75, line 8 and ending at line 25.

An output from the modulated-signal generator 10006 is a pulse-width-modulated signal (~~XDPi~~ XDPj) modulated to a pulse width corresponding to a luminance signal value. The modulated signal is input to the input terminal 71. The modulated signal is inverted by the inverter circuit 74 and input to the base of the transistor 75 such as a MOSFET to ON/OFF-control the transistor 75. When the modulated signal (~~XDPi~~ XDPj) is at high level, an output from the current source 72 is supplied to a modulated-signal wiring via the diode 73; when the modulated signal is at low level, the transistor 75 is turned on to flow a current from the current source 72 through the transistor 75 so as not to supply any current to the modulated-signal wiring. Note that the driving current output from the current source 72 is determined to a current value enough for the cold cathode device to emit electrons. For example, in Fig. 33, the driving current is determined to the device current If for a device voltage of 16V.

Please substitute the following paragraph for the paragraph starting at page 79, line 15 and ending at page 80, line 2.

An output from a modulated-signal generator 10006 is a pulse-width-modulated signal (~~XDPi~~ XDPj) modulated to a pulse width corresponding to a luminance signal value. The modulated signal is input to an input terminal 71. The modulated signal is inverted by an inverter circuit 74, and drives a transistor 75 such as a MOSFET to determine whether to flow an output current from a current source 72 to a modulated-signal wiring. When the modulated signal is at high level, the driving current is supplied to the modulated-signal wiring via a diode 73. This driving current is determined to a current enough for the cold cathode device to emit electrons. For example, in Fig. 33, the driving current is determined to the device current If for a device voltage of 16 V.

Please substitute the following paragraph for the paragraph starting at page 80, line 3 and ending at line 11.

The modulated signal (~~XDPi~~ XDPj) input to the input terminal 71 is also input to the first input terminal (706a) of the 5-input OR circuit 706. The second input terminal (706b) and third input terminal (706c) of the 5-input OR circuit 706 respectively receive the (j-2)th (second left) and (j-1)th (left) modulated signals. The fourth input terminal (706d) and fifth input terminal (706e) of the 5-input OR circuit 706 respectively receive the (j+1)th (right) and (j+2)th (second right) modulated signals.

Please substitute the following paragraph for the paragraph starting at page 80, line 12 and ending at line 23.

Similar to the fourth embodiment, the ~~first~~ second and ~~second~~ third input terminals of a 5-input OR circuit 706 and the fourth and fifth input terminals of a 5-input OR circuit 706 for modulated-signal wirings on the two ends are set to low level, and the ~~first~~ second input terminal of a 5-input OR circuit 706 and the fifth input terminal of a 5-input OR circuit 706 and the fifth input terminal of a 5-input OR circuit 705 for the second modulated-signal wirings from the two ends are also set to low level. Outputs from the 5-input OR circuits 706 are level-converted by level shift circuits 77, input to the bases of NPN transistors 78 which supply driving potentials to modulated-signal wirings via diodes 79 by emitter followers, respectively.

Please substitute the following paragraph for the paragraph starting at page 81, line 23 and ending at page 82, line 9.

A modulated signal (~~XDPi~~ XDPj) input to an input terminal 71 is input to the first input terminal (716a) of the 4-input OR circuit 716. The second input terminal 716(b) and third input terminal (~~716d~~ 716c) of the 4-input OR circuit 716 respectively receive the (j-1)th (left) and (j+1)th (right) modulated signals. Similar to the fourth and fifth embodiments, the input terminals of 4-input OR circuit 716 for modulated-signal wirings on the two ends, i.e., 4-input OR circuits 716 not having corresponding adjacent modulated signals are set to low level.

Further, in the sixth embodiment, the fourth input terminals (716d) of respective 4-input OR circuits 716 are commonly connected and receive a signal PPRE.

Please substitute the following paragraph for the paragraph starting at page 82, line 10 and ending at line 25.

As shown in Fig. 38, the signal PPRE changes to high level immediately before a modulated signal (~~XDPi~~ XDPj) rises to high level (active), i.e., at the start of the horizontal scanning period, and falls to low level simultaneously when the modulated signal reaches high level. For example, the signal PPRE rises 1 μsec before the modulated signal reaches high level, and falls to low level simultaneously when the modulated signal reaches high level. In Fig. 38, reference numeral 95 denotes crosstalk of the modulated signal X4 to the potential Vas; 96, crosstalk of the modulated signal X4 arising from the fall of the modulated signal X3 from the potential Vas to GND (which are the same as in the fourth and fifth embodiments); and 97, a state in which the potential of a modulated-signal wiring rises to the potential Vas before the modulated signal X4 arises.

Please substitute the following paragraph for the paragraph starting at page 85, line 17 and ending at line 21.

In Fig. 39, reference numeral 3902 denotes a switch for receiving a modulated signal and switching the output depending on the logic level of an input terminal 71; 3901, a switch for switching the output depending on an output from an OR circuit 7601; and 7601, a 2-input OR ~~switch~~ circuit.

Please substitute the following paragraph for the paragraph starting at page 86, line 1 and ending at line 17.

An output from a modulated-signal generator 10006 is a pulse-width-modulated signal (~~XDPi~~ XDPj) modulated to a pulse width corresponding to a luminance signal

value. The modulated signal is input to the input terminal 71. The modulated signal is input to the control terminal of the switch 3902 to control the switch 3902. When the modulated signal (XDPi) is at high level, the switch 3902 selects a node 3902a to supply an output from a current source 72 to a modulated-signal wiring; when the modulated signal is at low level, the switch 3902 selects a node 3902b to supply the potential GND as a reference potential or the potential Vas to the modulated-signal wiring. Note that the driving current output from the current source 72 is determined to a current value enough for the cold cathode device to emit electrons. For example, in Fig. 33, the driving current is determined to the device current If for a device voltage of 16 V.

Please substitute the following paragraph for the paragraph starting at page 86, line 18 and ending at page 87, line 4.

The first input terminal (~~76b~~ 7601a) and second input terminal (~~76c~~ 7601b) of the 2-input OR circuit ~~76~~ 7601 respectively receive the (j-1)th (left) and (j+1)th (right) modulated signals. The first or second input terminal of a 2-input OR circuit 7601 not having a left or right modulated signal is connected to GND, like 2-input OR circuits 7601 for modulated-signal wirings on the two ends which receive, e.g., signals X1 and X480. An output from the output terminal of the 2-input OR circuit7601 is input to the control terminal of the switch 3901. When the control terminal of the switch 3901 is at high level, the switch 3901 is connected to a node 3901a; when the control terminal is at low level, the switch 3901 is connected to a node 3901b.

Please substitute the following paragraph for the paragraph starting at page 88, line 6 and ending at line 18.

An output from a modulated-signal generator 10006 is a pulse-width-modulated signal (~~XDPi~~ XDPj) modulated to a pulse width corresponding to a luminance signal value. The modulated signal is input to an input terminal 71. The modulated signal is input to the control terminal of a switch 3902 to control the switch 3902. When the modulated signal is

at high level, the switch 3902 selects a node 3902a to supply an output from a current source 72 as a driving current to a modulated-signal wiring. Note that the driving current is determined to a current enough for the cold cathode device to emit electrons. For example, in Fig. 33, the driving current is determined to the device current If for a device voltage of 16 V.

Please substitute the following paragraph for the paragraph starting at page 88, line 19 and ending at line 25.

The first input terminal (~~706b~~ 70601a) and second input terminal (~~706c~~ 70601b) of the 4-input OR circuit 70601 respectively receive the (j-2)th (second left) and (j-1)th (left) modulated signals. The third input terminal (~~706d~~ 70601c) and fourth input terminal (~~706e~~ 70601d) of the 4-input OR circuit 70601 respectively receive the (j+1)th (right) and (j+2)th (second right) modulated signals.